

REMARKS

Claims 1-23 are all the claims pending in the application. By this Amendment, Applicant adds claims 24-28, which are clearly supported throughout the specification.

I. Summary of Office Action

Claims 2-12, 14, and 21-23 contain allowable subject matter. Claim 13 is rejected under double patenting obviousness rejection and claims 1, 15-17, 19, and 20 are rejected under 35 U.S.C. § 102.

II. Double Patenting Rejection

Claim 13 is rejected on the grounds of nonstatutory obviousness-type double patenting rejection over claim 28 of U.S. Patent No. 6,816,818 to Wolf et al. (hereinafter '818 patent). Applicant respectfully traverses these grounds of rejection in view of the following comments.

Independent claim 13 *inter alia* recites: “a first delay module delaying the at least one first clock signal by a first delay time; a second delay module delaying the second clock signal by a second delay time; and an adjustment module adjusting a phase of the second delay module, wherein the delayed, second clock signal is adapted to a phase of the delayed, at least one first clock signal.”

Claim 28 of the '818 patent recites:

A method of internal redundant clock distribution to synchronize an output signal of at least one receiver module with at least one external clock signal, comprising:

the at least one receiver module receiving at least one external clock signal;

distributing the external clock signal to at least a first independent clock signal generator module and a second independent clock signal generator module;

transmitting at least one item of master-slave status information about the first independent clock signal generator module and the second independent clock

signal generator module to the at least one receiver module;

regenerating the external clock signal by the first independent clock signal generator module and the second independent clock signal generator module;

transmitting the clock signals regenerated by the first independent clock signal generator module and the second independent clock signal generator module to the at least one receiver module;

selecting, as a function of the item of master-slave status information, at least one of the regenerated clock signals from the first independent clock signal generator module and the second independent clock signal generator module to serve as a master synchronization signal for the synchronization of the output signal of the at least one receiver module with the at least one external clock signal;

synchronizing the output signal of the at least one receiver module with the at least one regenerated clock signal selected as the master synchronization signal.

Claim 28 of the '818 patent does not disclose or even remotely suggest delaying the first and second clock signals *i.e.*, the first delay module and the second delay module, as set forth in claim 13. Furthermore, claim 28 of the '818 patent only discloses synchronizing the output signal with regenerated clock signal that is selected as the master synchronization signal. Claim 28 of the '818 patent does not disclose or even remotely suggest an adjustment module adjusting a phase of the second delay module. That is, claim 28 of the '818 patent does not disclose or even remotely suggest having the delayed, second clock signal is adapted to a phase of the delayed, at least one first clock signal. For at least these exemplary reasons, claim 13 is non obvious over claim 28 of the '818 patent. Applicant respectfully requests the Examiner to withdraw this double patenting rejection.

III. Claim Rejection - 35 U.S.C. § 102

Claims 1, 15-17, 19, and 20 are rejected under 35 U.S.C. § 102(b) as being anticipated by Hamamoto et al (US Patent 5,987,619). Applicant respectfully traverses this rejection in view of the following comments.

In general, the present invention relates to redundant internal clock generators because for purpose of internal redundancy, phase hits are not tolerated. In general, synchronous telecommunication equipment such as a digital cross-connect may have two redundant internal clock generators, which are typically both synchronized on the same external reference clock. Since such systems are of modular design, the modules need to be interconnected by internal cabling (electrical or optical).

In particular, each module (for example a matrix stage) must be supplied by both redundant clock generators to fully protect the function of the equipment. In this case, it is necessary that the two redundant clock signals, as these are received at the respective module, are phase aligned. In the conventional techniques, the use of matched cables of exactly the same length was required so that cable delay was the same for both redundant clock signals. In an exemplary embodiment of the present invention, however, this situation is improved by providing a fixed delay for the first clock signal. This fixed delay corresponds to the maximum allowable cable delay/length (*e.g.* 400 m). The second clock signal is delayed by a variable delay that corresponds to twice the maximum cable delay. This way, all possible cabling situations can be compensated for by using only one adjustable delay element and corresponding control instance. In other words, two delayed clock signals are phase adjusted to each other.

Accordingly, claim 1 *inter alia* recites “adjusting means for the phase adjustment of the second delay means, so that the delayed second clock signal is adapted to the phase of the

delayed first clock signal at an output end of the first delay means.” The Examiner contends that Hamamoto discloses these unique features of claim 1 (*see* page 4 of the Office Action). Applicant respectfully disagrees.

Hamamoto discloses an input signal phase compensation circuit with a clock signal generation circuit 7 connected to the clock signal input buffer 3 and two variable delay circuits 5 controlled by phase comparator 29 that are connected to clock signal generation circuit 7. Internal clock signal INTCLK is input to clock signal generation circuit 7, and clock signal FCLK in phase with internal clock signal INTCLK and clock signal BCLK phase shifted by 180 degrees are generated. These clock signals FCLK and BCLK are input to corresponding variable delay circuits 5 and delayed by time Dv. Hamamoto further discloses signals output from variable delay circuits 5 are delayed time Dp by wiring resistances 9, 11, and clock signals FDCLK and BDCLK are generated. In Hamamoto, however, there is no disclosure or suggestion that the clock signals FCLK and BCLK (*alleged* first and second clock signals) are phase adjusted (Figs. 7 and 8A to 8H; col. 6, lines 11 to 39).

In Hamamoto, the clock signal FDCLK is input to the phase comparator 29 which compares its phase with the phase of monitored write data signal MWD. The phase comparator 29 determines common time Dv for delaying respective clock signals FCLK and BCLK in two variable delay circuits 5 so as to match phases of clock signal FDCLK and monitored write data signal MWD (Fig. 7; col. 6, lines 11 to 54). In other words, Hamamoto discloses a phase comparator 29 which compares the phases of a delayed internal clock signal and a monitored write data signal MWD and controls the variable delays such that the clock signal is synchronized with the data signal. In Hamamoto, the phase comparator 29 (*alleged* adjusting

means) does not adjust the variable delay circuit 5 so that the delayed FCLK adopts the phase of the delayed BCLK. In fact, it is explicitly disclosed that the BCLK is phase shifted to the FCLK.

The Examiner contends that Figs. 7, 8, 9, 10, and 11 disclose the above-quoted unique features of claim 1 (*see* page 4 of the Office Action). Applicant has already demonstrated that Figs. 7 and 8 that relate to the second embodiment do not disclose or suggest the unique features of claim 1. Figs. 9-11 relate to two other different embodiments of Hamamoto (third and fourth embodiments). Applicant respectfully notes that the Examiner may not combine features from different embodiments without motivation to do so. *In re Kramer*, 18 USPQ2d 1415, 1416 (Fed. Cir. 1991).

Therefore, “adjusting means for the phase adjustment of the second delay means, so that the delayed second clock signal is adapted to the phase of the delayed first clock signal at an output end of the first delay means,” as set forth in claim 1 is not disclosed by Hamamoto, which lacks having the phase comparator 29 adjust the phase of the delayed BCLK signal to the phase of the FCLK signal or vice versa. For at least these exemplary reasons, claim 1 is patentably distinguishable from Hamamoto. Accordingly, Applicant respectfully requests the Examiner to withdraw this rejection of claim 1.

Independent claim 15 recites features similar to, although not necessarily coextensive with, the features argued above with respect to claim 1. Therefore, arguments presented with respect to claim 1 are respectfully submitted to apply with equal force here. For at least substantially analogous exemplary reasons, therefore, independent claim 15 is patentably

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distinguishable from Hamamoto. Claims 16, 17, 19, and 20 are patentable by virtue of their dependency on claim 1 or 15.

IV. Allowable Subject Matter

Applicant thanks the Examiner for allowing claims 2, 10, 14, 18, 21, and 22. Applicant further thanks the Examiner for indicating that claims 3-9, 11, 12, and 23 contain allowable subject matter. Applicant does not acquiesce to the Examiner's reasons for allowance.

V. New Claims

In order to provide more varied protection, Applicant adds claims 24-28, which are patentable at least by virtue of their dependency on claim 1, 13, or 15.

VI. Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly invited to contact the undersigned attorney at the telephone number listed below.

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